SPECIFICATIONS AND FEATURES

DATASHEET

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UFirebird IV-UC7510

Multi-GNSS Single-Frequency Positioning Chip

Foreword

About This Document

This datasheet offers you information in the functional characteristics, hardware features, electrical specifications, mechanical specifications, etc. of Unicore UC7510 chip.

Target Readers

This datasheet is intended for technical personnel familiar with GNSS receivers.

Statement

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Revision History

Version	Revision History	Date
R1.0	First release.	Feb. 2026

Document Status

Releases	Status Descriptions	Current Status
Primary	This is a pre-release version with target specifications that are subject to revision.	
Alpha release	This is an alpha release version, which has been preliminarily tested and verified. The content may undergo minor modifications based on user feedback and further testing.	
Production release	The document contains the complete and final specifications.	√

1 Functional Characteristics

1.1 Overview

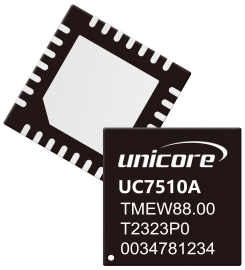


Figure 1-1 UFirebird IV-UC7510 Chip

Unicore UFirebird IV™ chip (see Product Models of UC7510) features 22 nm process with low power consumption and ultra-small form factor, significantly increasing the battery life of users' device.

UC7510 is suitable for global applications. It supports L1 band of GPS, GLONASS, BDS, Galileo and QZSS multi-constellation joint positioning, and supports the reception and processing of multiple SBAS signals, providing users with fast, accurate and high-performance positioning experience.

UC7510 is highly integrated, with built-in LDO, LNA, RTC, etc. It can provide the function of a complete GNSS receiver with only a few external components, significantly reducing the PCB area and hardware costs for users.

The sub-model UC7510A-01 supports connection of various sensors such as gyroscopes, accelerometers, and odometers for fusion positioning. With the built-in DR (dead reckoning) algorithm, the chip can directly output GNSS + MEMS integrated positioning results, enabling continuous positioning even in tunnels and underground garages.

UC7510 chips use QFN28 package, and the automotive-grade chips are qualified according to AEC-Q100 (Grade 2).

Table 1-1 Product Models of UC7510

Product Model	Grade	Package	Feature
UC7510A-00	Automotive	QFN28	SPP
UC7510A-01	Automotive	QFN28	SPP + DR
UC7510A-02	Automotive	QFN28	SPP + RawData
UC7510I-00	Industrial	QFN28	SPP

Product Model	Grade	Package	Feature
UC7510I-02	Industrial	QFN28	SPP + RawData

1.2 Features

UC7510 has the following features:

- Positioning engine
  - 64 channels concurrently tracking signals
  - Less than 1 second hot start time
  - -148 dBm cold start sensitivity, -165 dBm tracking sensitivity
  - Up to 10 Hz data update rate
- Supports GPS, BDS, GLONASS, Galileo and QZSS
- Supports external connection of 26 MHz TCXO
- Supports external connection of 32.768 kHz crystal
- Built-in flash, supporting firmware upgrade
- Automotive grade and industrial grade, 4.0 mm × 4.0 mm, QFN28 package

1.3 Performance

The performance of UC7510 is as follows:

Table 1-2 UC7510 Performance

Item	Description
Positioning accuracy (single point positioning)[1]	< 2.0 m
Velocity accuracy[2]	0.05 m/s
GNSS positioning data update rate	Up to 10 Hz
Raw data output rate	RTCM up to 10 Hz
Sensitivity[3]	GNSS Tracking: -165 dBm Reacquisition: -160 dBm Cold start: -148 dBm

Item	Description
	Hot start: -156 dBm
TTFF[4]	GNSS Cold start: < 26 s AGNSS[5]: < 3 s Hot start: < 1 s Reacquisition: < 1 s
Operational limits	Altitude: -2000 m ~ 18000 m Velocity: 515 m/s Dynamics: 4 g

[1] CEP50, open sky.

[2] 68% at 30 m/s for dynamic operation, open sky.

[3] A good external LNA is required to ensure the performance.

[4] Satellite signal strength needs to achieve -130 dBm.

[5] Timely injection of assistance data.

1.4 Block Diagram

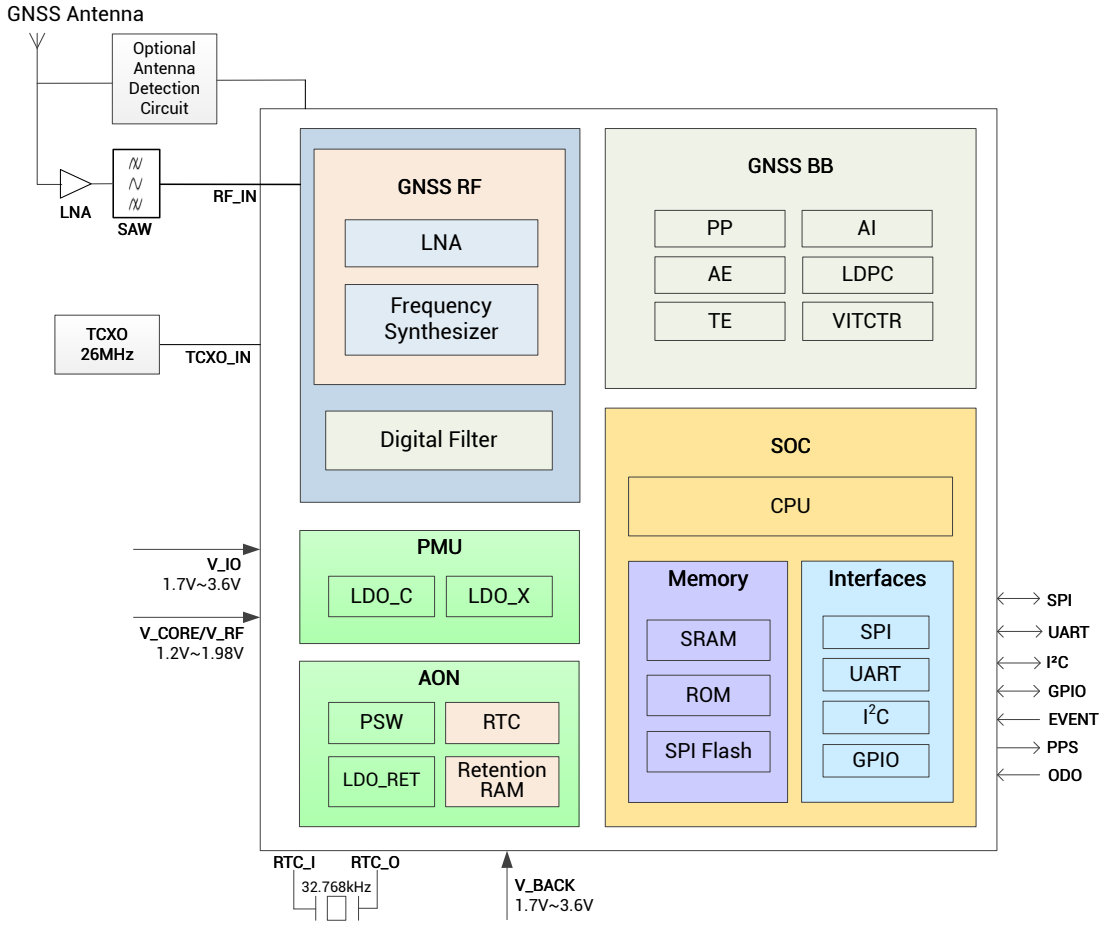


Figure 1-2 UC7510 Chip Block Diagram

> **Note:** The SPI interface is shared with the UART and I2C interface pins. When using SPI, UART and I2C are unavailable.

1.5 Supported GNSS

UC7510 supports multiple GNSS joint positioning, including GPS L1, BDS B1, GLONASS L1, Galileo E1 and QZSS L1. The RF uses a wideband design that can simultaneously receive and process GPS, BDS, GLONASS, Galileo and QZSS signals.

Table 1-3 Supported GNSS and Frequencies

GNSS	Frequency
GPS	L1C/A (1575.42 MHz)
BDS	B1I (1561.098 MHz) B1C (1575.42MHz)

GNSS	Frequency
GLONASS	G1 (1602 MHz + k*562.5 KHz，k=-7~+6)
Galileo	E1B/C (1575.42 MHz)
QZSS	L1C/A, L1C/B, L1S (1575.42 MHz)

> **Note:** QZSS is supported only when GPS is enabled.

1.6 Protocols

The UC7510 protocol complies with NMEA 4.11 and "Unicore Protocol" specification. By default, UC7510 communicates with the host device via UART. For the message structures, parameters, communication interfaces and firmware versions, please refer to *UFirebirdIV Series Protocol Specification*.

1.6.1 Terms and Abbreviations

The following table lists the terms and abbreviations involved in this document:

Table 1-4 Terms and Abbreviations

Abbreviation	Complete Name
A/D	Analog/Digital
ADC	Analog Digital Convertor
AGC	Automatic Gain Control
AGNSS	Assisted GNSS
AON	Always ON
BB	Baseband
DGNSS	Differential GNSS
Galileo	Galileo Navigation Satellite System
GLONASS	Global Navigation Satellite System
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
BDS	BeiDou Navigation Satellite System

Abbreviation	Complete Name
LDO	Low DropOut regulator
LNA	Low Noise Amplifier
ODO	Odometer
OSC	Oscillator
PGA	Programmable Gain Amplifier
PIO	Programming Input/Output
PLL	Phase Locked Loop
PMU	Power Management Unit
POR	Power-on Reset
PSW	Power Switch
RAM	Random Access Memory
RF	Radio Frequency
RTC	Real-Time Clock
SBAS	Satellite-Based Augmentation System
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
TCXO	Temperature Compensate Crystal Oscillator
SPP	Single Point Positioning
DR	Dead Reckoning

2 RF Subsystem

The RF subsystem amplifies the received RF signals to the proper levels, and then down-converts the RF signals to IF bands. After A/D conversion, the GNSS signals are sent to the baseband section. During this process, the LNA integrated in UC7510 provides low-noise amplification and it requires external matching for normal operation. For applications which require high performance, an external LNA is recommended, and its gain range is recommended to be within 17 dB ~ 45 dB. Furthermore, it is necessary to use an external SAW filter to reduce the interference out of the GNSS band.

3 Baseband Subsystem

3.1 Interfaces

The digital I/Os of the baseband part are powered by V_IO, and the level of V_IO is the same as the logic voltage level. Without supplying V_IO, the UC7510 chip will not work.

3.1.1 UART

UC7510 provides one UART interface, which can be used for communication with a host. This interface supports configurable baud rates up to 921600 bps.

By default, PIO0 and PIO1 correspond to UART, and the interface can be mapped to other PIOs via D_SEL0 and D_SEL1. PIO0 and PIO1 can also be used as I2C, in which case the UART will be mapped to PIO2 and PIO3. For more information about the use of D_SEL, see D_SEL0 / D_SEL1 Interface Configuration.

The parameters of UART are listed below.

Table 3-1 UART Parameters

Symbol	Parameter	Min	Max	Unit
R_u	Baud rate	9600	921600	Bit/s
Δ_{Tx}	TX baud rate accuracy	-0.5%	+0.5%	/
Δ_{Rx}	RX baud rate tolerance	-2%	+2%	/

3.1.2 I2C

UC7510 provides an I2C interface, which is enabled by default and corresponds to PIO2 and PIO3. It can be mapped to PIO0 and PIO1 via D_SEL0 and D_SEL1, in which case the PIO2 and PIO3 will be used as UART, as shown in D_SEL0 / D_SEL1 Interface Configuration.

> **Note:** UC7510A-01 defaults to using PIO2 and PIO3 as the I2C interface to connect to the IMU and does not support user configuration.

The timing requirements of I2C are as follows:

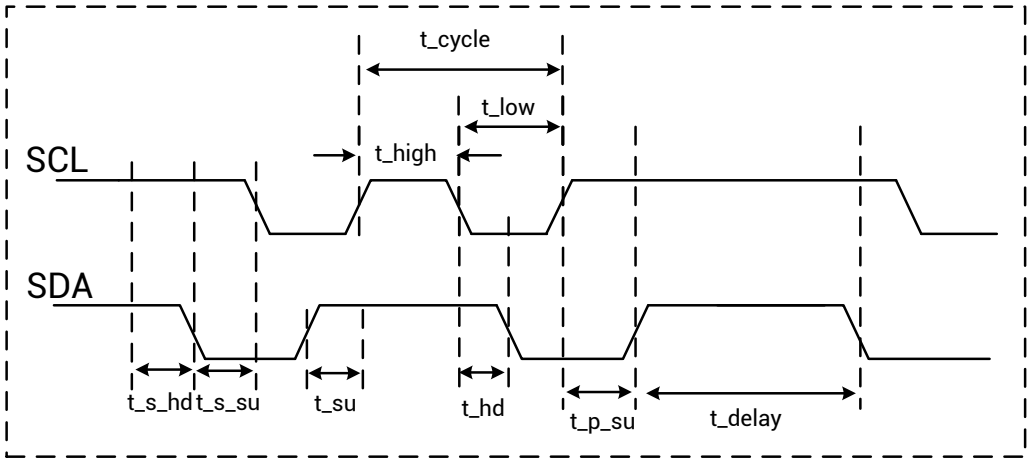


Figure 3-1 I2C Timing Requirements

Table 3-2 I2C Timing Requirements

No.	Parameter	Parameter Description	Min.	Max.	Unit
1	t_cycle	SCL clock period	100	3400	kbps
2	t_high	High period of SCL clock	0.06	5	us
3	t_low	Low period of SCL clock	0.16	5	us
4	t_su	Data setup time	0.072	/	us
5	t_hd	Data hold time	0.072	/	us
6	t_s_su	Setup time for start condition	0.072	/	us
7	t_s_hd	Hold time for start condition	0.072	/	us
8	t_p_su	Setup time for stop condition	0.072	/	us
9	t_delay	Delay time between a start and stop condition	0.5	/	us

3.1.3 SPI Slave

UC7510 provides an SPI Slave interface, which supports a maximum communication speed of 24 MHz. This interface is disabled by default and can be mapped to PIO0, PIO1, PIO2 and PIO3 via D_SEL0 and D_SEL1, sharing pins with I2C and UART, as shown in D_SEL0 / D_SEL1 Interface Configuration.

3.1.4 SPI Master

UC7510 provides an SPI Master interface, which supports a maximum communication speed of 24 MHz. This interface is disabled by default and can be mapped to PIO0, PIO1, PIO4 and PIO5 (or PIO2, PIO3, PIO4 and PIO5), as shown in PIO Functions.

3.1.5 SPI Flash

UC7510 provides an SPI interface to communicate with external Flash, which supports a maximum communication speed of 24 MHz. This interface is disabled by default and can be mapped to PIO2, PIO3, PIO6 and PIO7 via D_SEL0 and D_SEL1, as shown in D_SEL0 / D_SEL1 Interface Configuration.

3.1.6 Odometer

UC7510 provides an odometer interface to receive the odometer direction signal (ODO_DIR) and odometer pulse signal (ODO_PULSE). The ODO_DIR is input through PIO9 and the ODO_PULSE is input through PIO8.

The input signals need to meet the requirements of V_{il} and V_{ih} specified in PIO Specifications, which are listed below for the convenience of viewing.

Table 3-3 Requirements for the Odometer Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{il}	Low level input voltage	/	/	0.2×V_IO	V
V_{ih}	High level input voltage	0.8×V_IO	/	/	V

The default configuration of the odometer direction signal is

- forward at high level
- reverse at low level

The above configuration can be changed using the **CFGODOFWD** command. For more information about the command, please refer to *UFirebird IV Protocol Specification*.

The odometer pulse signal needs to meet the following requirements:

1. The odometer pulse is required to be a square wave signal with a frequency not higher than 10 KHz.
2. The distance corresponding to a square wave signal is required to be between 1 cm and 27 cm. For example, if the distance is 20 cm, the output frequency is

   f = [(1000/20) * V/36] Hz

where V is the velocity of the vehicle and its unit is km/h.

3. The chip detects the number of rising edges of the square wave signal, and both high-level and low-level durations are required to be no less than 100 μs.

4. If the vehicle is stationary (for example, parking), the voltage level of ODO_PULSE pin must remain constant.

3.2 PIO

The PIO block can be used as GPIO or the aforementioned interfaces. The following table describes all PIO functions.

Table 3-4 PIO Functions

PIO #	Default Function	I/O	Description	Alternate Function
0	GPIO0	I/O	/	UART_RX I2C_SDA SPIS_MOSI SPIM_MOSI
1	GPIO1	I/O	/	UART_TX I2C_SCL SPIS_MISO SPIM_MISO
2	GPIO2	I/O	/	I2C_SDA UART_RX SPIS_CSN SPIM_MISO SPIF_CSN
3	GPIO3	I/O	/	I2C_SCL UART_TX SPIS_CLK SPIM_MOSI SPIF_CLK
4	GPIO4	I/O	/	PPS SPIM_CSN
5	GPIO5	I/O	/	EVENT SPIM_CLK
6	GPIO6	I/O	D_SEL0 is used for interface selection of UART, I2C and SPI. For more information, see D_SEL0 / D_SEL1 Interface	D_SEL0 SPIF_TxRx[0]

PIO #	Default Function	I/O	Description	Alternate Function
			Configuration.	
7	GPIO7	I/O	D_SEL1 is used for interface selection of UART, I2C and SPI. For more information, see D_SEL0 / D_SEL1 Interface Configuration.	D_SEL1 SPIF_TxRx[1]
8	GPIO8	I/O	/	ODO_PULSE
9	GPIO9	I/O	/	ODO_DIR

Table 3-5 D_SEL0 / D_SEL1 Interface Configuration

D_SEL0 (PIO6)	D_SEL1 (PIO7)	Interface	Pin	PIO
0 or pull down	0 or pull down	UART	RX	PIO0
			TX	PIO1
		I2C	SDA	PIO2
			SCL	PIO3
1 or pull up	0 or pull down	UART	RX	PIO2
			TX	PIO3
		I2C	SDA	PIO0
			SCL	PIO1
0 or pull down	1 or pull up	SPI Slave	MOSI	PIO0
			MISO	PIO1
			CSN	PIO2
			CLK	PIO3
1 or pull up	1 or pull up	UART	RX	PIO0
			TX	PIO1
		SPI Flash	CSN	PIO2
			CLK	PIO3
			TxRx[0]	PIO6
			TxRx[1]	PIO7

> **Note:** UC7510A-01 defaults to using PIO2 and PIO3 as the I2C interface to connect to the IMU and does not support user configuration.

Table 3-6 PIO State After Power-On

PIO #	When RESET_N is low	When RESET_N is high, it enters Boot ROM mode, and waits for a firmware update request.				When RESET_N is high, if no firmware update request is detected, it proceeds to firmware execution.
		D_SEL0==0 D_SEL1==0	D_SEL0==1 D_SEL1==0	D_SEL0==0 D_SEL1==1	D_SEL0==1 D_SEL1==1	
0	GPIO, input with weak pull-up	UART RX, input with weak pull-up	I2C SDA, input with weak pull-up	SPIS_MOSI, input with weak pull-up	UART RX, input with weak pull-up	Depending on the firmware
1	GPIO, input with weak pull-up	UART TX, output	I2C SCL, input with weak pull-up	SPIS_MISO, input with weak pull-up oroutput	UART TX, output	Depending on the firmware
2	GPIO, input with weak pull-up	I2C SDA, input with weak pull-up	UART RX, input with weak pull-up	SPIS_CSN, input with weak pull-up	SPIF_CSN, output high level	Depending on the firmware
3	GPIO, input with weak pull-up	I2C SCL, input with weak pull-up	UART TX, output	SPIS_CLK, input with weak pull-up	SPIF_CLK, output high level	Depending on the firmware
4	GPIO, input with	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	Depending on the firmware

PIO #	When RESET_N is low	When RESET_N is high, it enters Boot ROM mode, and waits for a firmware update request.				When RESET_N is high, if no firmware update request is detected, it proceeds to firmware execution.
		D_SEL0==0 D_SEL1==0	D_SEL0==1 D_SEL1==0	D_SEL0==0 D_SEL1==1	D_SEL0==1 D_SEL1==1	
	weak pull-up					
5	GPIO, input with weak pull-down	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, output low level	GPIO, input with weak pull-up	Depending on the firmware
6	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	SPIF_TxRx[0], input with weak pull-up or output	Depending on the firmware
7	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	SPIF_TxRx[1], input with weak pull-up or output	Depending on the firmware
8	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	Depending on the firmware
9	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	GPIO, input with weak pull-up	Depending on the firmware

3.3 Watchdog

UC7510 includes a watchdog timer, which prevents system-lockups caused if the software gets trapped in a deadlock. During normal operation, the firmware resets the watchdog's internal counter at regular intervals before the timer overflow occurs.

3.4 Timer Counter

The timer counter supports a TIMEMARK input (EVENT) and a TIMEPULSE output (PPS).

The TIMEMARK can be input via PIO5 and it is an external timestamp event relative to GPS time.

The TIMEPULSE can be output via PIO4, but only one TIMEPULSE can be output at a time. The output pulses are synchronized with GPS or UTC time grid, and the time interval can be configured over a wide range of frequency.

3.5 Clock

3.5.1 TCXO

UC7510 requires an external 26 MHz clock, which can be provided by a TCXO, to supply the reference frequency for the RF and the baseband PLL.

3.5.2 PLL

The fully integrated, low-power PLL generates the system clock from the 26 MHz reference frequency supplied by the TCXO.

3.5.3 RTC

The RTC is driven internally by a 32.768 kHz oscillator, which makes use of an external 32.768 kHz crystal.

If the main power supply and the IO power supply fail and a backup battery is connected to V_BACK, the baseband, RF and CPU switch off, but the RTC still runs to provide a timing reference for the receiver. This operating mode is called RTC time keeping mode. Under this mode, the relevant data are saved in the flash.

The RTC time keeping mode is a prerequisite for GNSS hot start. If the RTC is abnormal, it will affect the performance of hot start.

If the RTC time keeping mode is not used, the backup battery is unnecessary, and V_BACK needs to be connected to ground or to V_IO. When RTC is not used, the RTC_I pin needs to be connected to ground and RTC_O can be left open.

By default, the standard firmware supports 32.768 kHz crystal. Besides, UC7510 also supports an external digital clock signal of 32.768 kHz directly input into the RTC_I pin to replace the crystal, and the RTC_O should be open. When using the external digital clock signal, please note that the signal amplitude should be higher than 2 V and lower than Min (V_IO, V_BACK)[1], otherwise it may cause damage to the components of UC7510.

[1] The voltages of V_IO and V_BACK need to be higher than 2 V.

3.5.4 Clock Source Combination

Table 3-7 Clock Source Combination

Main clock input	RTC clock input	Description
26 MHz TCXO connected to TCXO_IN	32.768 kHz crystal connected to RTC_I and RTC_O	Normal use; a backup battery is needed to supply V_BACK to keep the RTC running.
26 MHz TCXO connected to TCXO_IN	32.768 kHz external digital signal connected to RTC_I; RTC_O open	Normal use; a backup battery is needed to supply V_BACK to keep the RTC running.
26 MHz TCXO connected to TCXO_IN	No clock input; RTC_I connected to ground; RTC_O open	GNSS hot start is not supported in this condition.

For the application with the above clock source combination, please note the followings:

- When using the 26 MHz TCXO, it can be powered by LDO_X or an external power source.
- When the 32.768 kHz external digital signal is used as the RTC clock, its waveform amplitude should be higher than 2 V and lower than Min (V_IO, V_BACK)[1], and the clock drift should be within ±0.6 Hz, 20 ppm.

[1] The voltages of V_IO and V_BACK need to be higher than 2 V.

4 Operating Modes

4.1 Continuous Tracking Mode

Under the full-speed operation mode, the chip's hardware keeps tracking and processing satellite signals without interruption to ensure the positioning performance, velocity accuracy and TTFF with high-quality signal acquisition and tracking.

4.2 Sleep Mode

In the sleep mode, the chip is in power-off state except for the RTC time keeping unit and the Retention RAM. Users can wake up the chip according to actual needs. The chip runs at a very low power level in the sleep mode and can quickly enter into hot start after waking up.

5 System Configuration

5.1 Configuring the Communication Interface

UC7510 has one UART, one I2C and one SPI interface. The SPI interface is shared with the UART and I2C interface pins. When using SPI, UART and I2C are unavailable.

Users can select the function of the communication interfaces with D_SEL0 and D_SEL1. For more information, see D_SEL0 / D_SEL1 Interface Configuration.

5.2 Configuration Pins

There are two configuration pins: PIO6 (D_SEL0) and PIO7 (D_SEL1). D_SEL0 and D_SEL1 are the latch values of PIO6 and PIO7 respectively, at the moment when the chip is powered up and RESET_N changes from low to high. After RESET_N is high, the values of D_SEL0 and D_SEL1 remain unchanged inside the chip, and PIO6 and PIO7 can be configured for other functions. When the chip is powered up, PIO6 and PIO7 should be pulled up or pulled down according to the actual application requirements. For more information, see D_SEL0 / D_SEL1 Interface Configuration.

5.3 System Reset

The chip supports two types of reset: external reset and internal reset.

1. External reset: The chip is reset through the pin RESET_N.
2. Internal reset: The chip is reset by the internal POR when all power supplies are powered up or down.

5.4 Power Management

The PMU (Power Management Unit) provides 5 power domains that are internally generated by LDOs and supervised by several voltage monitors:

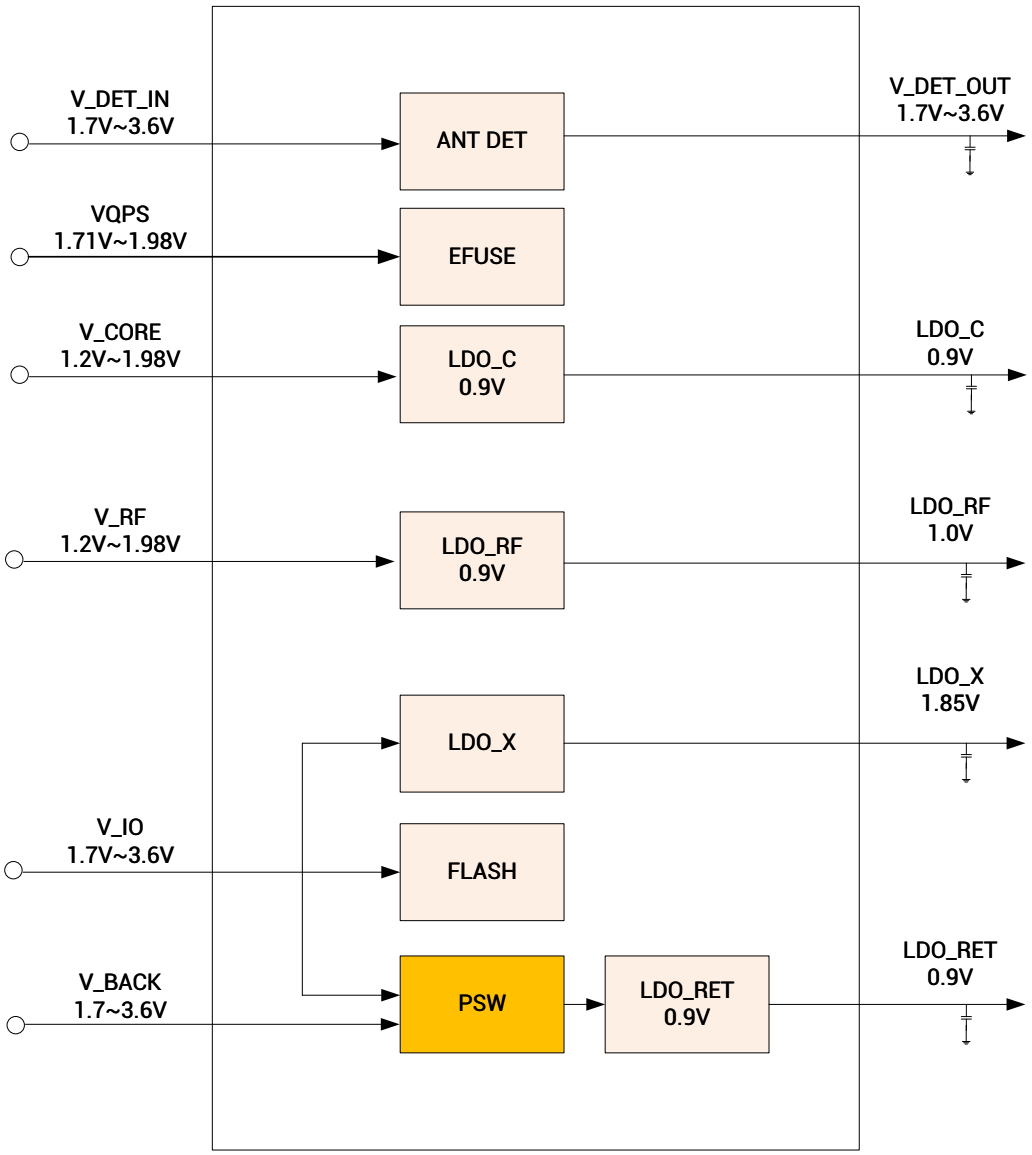


Figure 5-1 Power Management Unit

Core

The Core power domain is the main power domain for the digital section of the chip, powered by V_CORE. The subsequent LDO_C converts the V_CORE input to 0.9 V, which is output through the LDO_C pin. The LDO_C pin is connected to a decoupling capacitor. LDO_C drives the digital logic components.

RF

The RF power domain is the main power domain for the RF section of the chip, powered by V_RF. The subsequent LDO_RF converts the V_RF input to 1.0 V, which is output through the LDO_RF pin. The LDO_RF pin is connected to a decoupling capacitor. LDO_RF drives the RF logic components.

IO

The IO power domain is powered by V_IO, driving the chip IO components and on-chip Flash. The voltage supply of V_IO is 1.7 V to 3.6 V.

Backup

The Backup power domain runs the RTC section and Retention RAM. This domain is powered by V_IO and V_BACK. When the voltage of V_IO is normal, it uses V_IO, otherwise uses V_BACK. The allowed range of V_BACK is 1.7 V to 3.6 V. If the RTC and backup function are not needed, please connect the V_BACK pin to V_IO or ground.

TCXO

The clock power domain supplies power to TCXO. This domain has a dedicated LDO called LDO_X, which is also powered by V_IO. If the TCXO is powered by LDO_X, LDO_X should be connected to the power supply pin of the TCXO and decoupled with a capacitor. Alternatively, users may choose an external supply instead of the LDO_X to power TCXO.

Based on the above division of power domains and hardware design, UC7510 supports three modes of power consumption:

- Running mode: Every power source of the chip is normal, CPU runs normally, and the power supply of each domain is set by the software. All events, including external interruption, communication request, timing, etc., can be processed normally.
- V_BACK mode: The IO and main power supply of the chip is cut off from the outside, leaving only V_BACK powered. In this state, the power consumption of the chip drops to a very low level, with specific functions and power consumption depending on the software configuration for this mode. The chip wakes up immediately upon power-on.
- Power off mode: All power supplies are cut off from the outside, and the chip does not work at all.

5.5 Power-On and Power-Off Requirements

V_IO should be powered up no later than V_CORE/V_RF (no requirement for time interval), and its power-up time should be less than 10 ms.

V_CORE and V_RF must be used together and powered up at the same time. The power-up time difference between the two should be no more than 0.6 ms, and the power-up time should be less than 10 ms.

There is no requirement for the power up of V_BACK.

V_BACK is usually supplied by a backup battery, and it only supplies power to the AON area. When both V_IO and V_BACK are supplied, the AON area uses power from V_IO. Only when V_IO is powered off, the AON area switches to using V_BACK, which minimizes the consumption of the backup battery. The power supply is controlled by the power switch (PSW) inside the AON area.

The AON area works normally when power is supplied to either of V_IO or V_BACK. If neither V_IO nor V_BACK is powered, the AON area does not work. If power is supplied to any of the pins, the AON area will be reset and start working soon.

The power-up and power-down requirements are shown below.

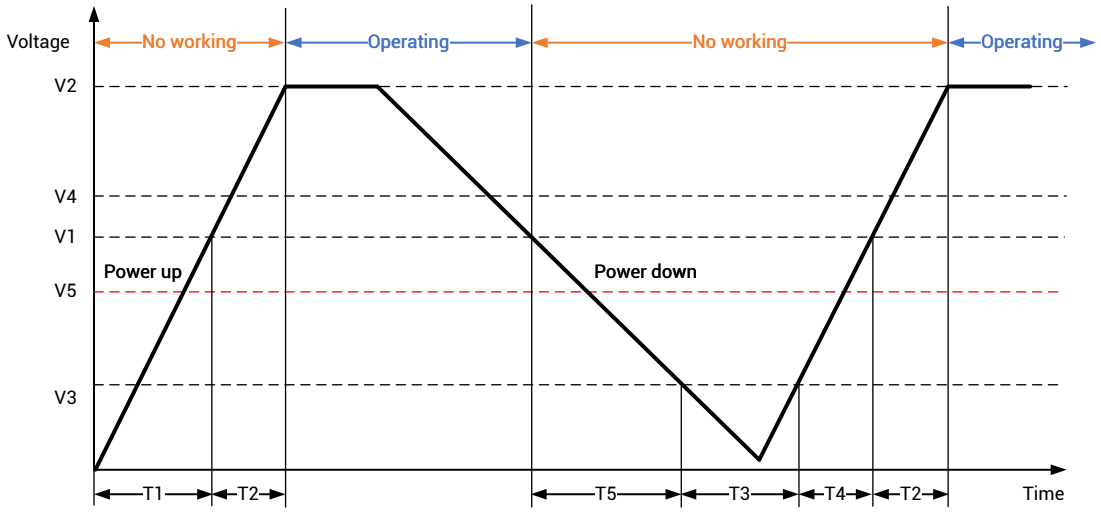


Figure 5-2 Power-up and Power-down Requirements

Table 5-1 Power-up and Power-down Requirements

	V_IO	V_CORE/ V_RF	V_BACK
Minimum operating voltage (V1)	1.70 V	1.20 V	1.70 V
Operating voltage (V2)	≤ 3.6 V	≤ 1.98 V	≤ 3.6 V
Restart threshold voltage (V3)	< 0.4 V	< 0.4 V	< 0.4 V (If V_BACK is connected to a backup power supply, there is no need to power down V_BACK. If V_BACK is connected to V_IO, the requirement for V_BACK is the same as that of V_IO. If V_BACK is connected to GND,

	V_IO	V_CORE/ V_RF	V_BACK
			there is no requirement.)
Memory holding voltage (V4)	N/A	N/A	> 1.7 V
RESET_N voltage (V5)	≥ (V_IO/2) + 0.4 V	N/A	N/A
Initial power supply rise time (T1)	> 100 µs	> 100 µs	> 100 µs
Operation start time (T2)	< 10 ms	< 10 ms	< 10 ms
Restart threshold voltage holding time (T3)	> 10 ms	> 10 ms	> 10 ms
Reboot power rise time (T4)	> 100 µs	> 100 µs	> 100 µs
Decay time (T5)	> 10 ms (affected by capacitance)	> 10 ms (affected by capacitance)	> 10 ms (affected by capacitance)
T_{up} (T1 + T2)	100 µs ~ 10 ms	100 µs ~ 10 ms	100 µs ~ 10 ms
T_{wait} (T5 + T3 + T4)	> 10 ms (T5 affected by capacitance)	> 10 ms (T5 affected by capacitance)	> 10 ms (T5 affected by capacitance)

6 Pin Definition

6.1 Pin Assignment

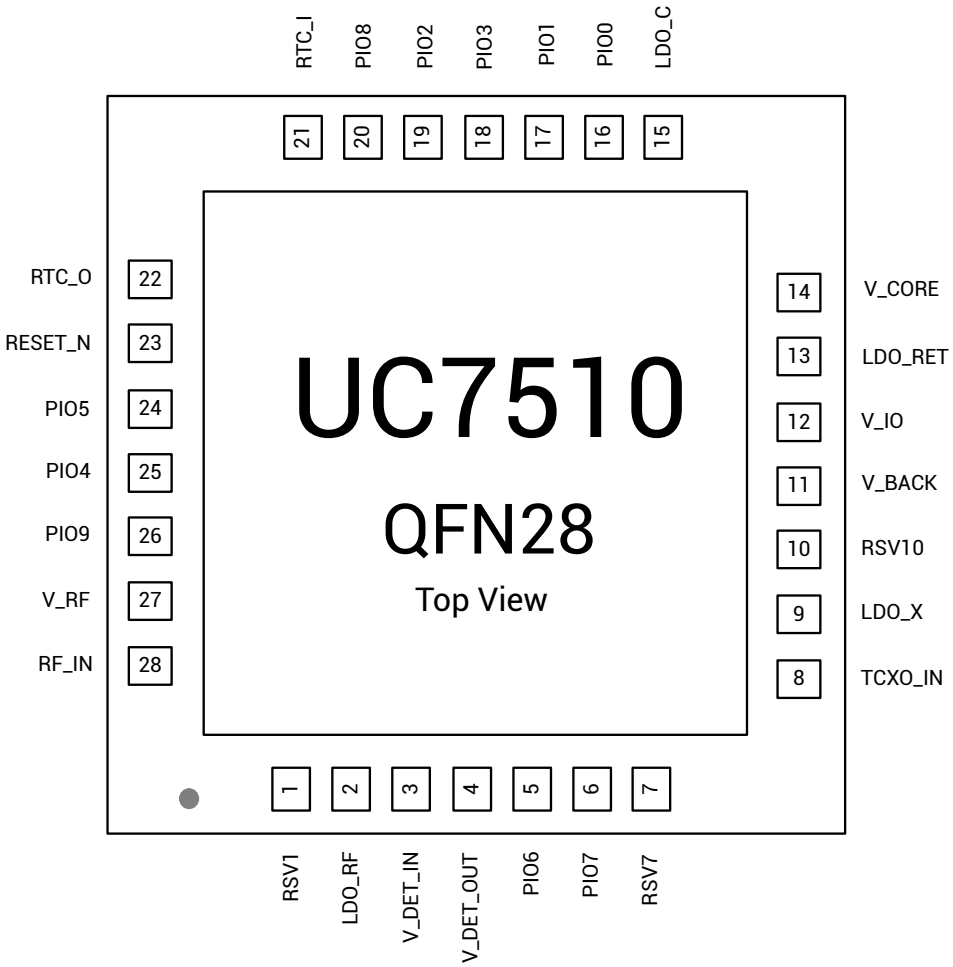


Figure 6-1 QFN28 Pin Assignment

6.2 Pin Description

Table 6-1 Pin Description

No.	Name	I/O	Description
1	RSV1	/	Leave open
2	LDO_RF	O	RF LDO output (external capacitor to GND is required)
3	V_DET_IN	I	Antenna detection power input (connect to GND or leave open if not used)

No.	Name	I/O	Description
4	V_DET_OUT	O	Antenna detection power output (leave open if not used)
5	PIO6	I/O	D_SEL0 (interface selection of UART, I2C and SPI) / SPIF TxRx[0] / GPIO6
6	PIO7	I/O	D_SEL1 (interface selection of UART, I2C and SPI) / SPIF TxRx[1] / GPIO7
7	RSV7	/	Connect to GND
8	TCXO_IN	I	26 MHz TCXO input
9	LDO_X	O	LDO output for TCXO
10	RSV10	/	Connect to GND
11	V_BACK	I	Backup battery input (connect to GND or V_IO when RTC time keeping mode is not used)
12	V_IO	I	IO power supply input
13	LDO_RET	O	LDO output for RTC time keeping (external capacitor to GND is required)
14	V_CORE	I	Core power supply input
15	LDO_C	O	Core LDO power supply output (external capacitor to GND is required)
16	PIO0	I/O	RX / SDA / SPIS MOSI / SPIM MOSI / GPIO0
17	PIO1	I/O	TX / SCL / SPIS MISO / SPIM MISO / GPIO1
18	PIO3	I/O	SCL / TX / SPIS CLK / SPIM MOSI / SPIF CLK / GPIO3
19	PIO2	I/O	SDA / RX / SPIS CS / SPIM MISO / SPIF CSN / GPIO2
20	PIO8	I/O	Odometer pulse signal input (leave open if not used) / GPIO8
21	RTC_I	I	32.768 kHz crystal input (connect to GND if not used)
22	RTC_O	O	32.768 kHz crystal output (leave open if not used)
23	RESET_N	I	System reset (active low for at least 1 ms to trigger a reset)
24	PIO5	I/O	External event input / SPIM CLK / GPIO5
25	PIO4	I/O	Pulse per second / SPIM CSN / GPIO4
26	PIO9	I/O	Odometer direction signal input (leave open if not used) /

No.	Name	I/O	Description
			GPIO9
27	V_RF	I	RF power supply input (voltage same as V_CORE)
28	RF_IN	I	RF signal input (LNA requires an external input matching)

7 Electrical Specifications

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Condition
V_CORE	LDO_C input voltage	-0.2	1.98	V	/
V_RF	LDO_RF input voltage	-0.2	1.98	V	/
V_IO	IO, LDO_X and AON PSW input voltage	-0.2	3.6	V	/
V_BACK	AON PSW input voltage	-0.2	3.6	V	/
V_DET_OUT	Antenna detection output voltage	-0.2	3.6	V	/
V_DET_IN	Antenna detection input current	/	100	mA	/
Vi_{tcxo}	TCXO_IN input voltage	-0.2	1.98	V	/
Vi_{ana}	RTC_I input voltage	-0.2	3.6	V	/
Vi_{dig}	PIO 0-9 and RESET_N input voltage	-0.2	3.6	V	/
P_{rfin}	RF input power at RF_IN	/	+10.5	dBm	1.06 V sinusoidal signal @ 50 Ω
P_{tot}	Total power	/	180	mW	105°C
T_{jun}	Junction temperature	-40	+125	°C	/
T_s	Storage temperature	-50	+150	°C	/
ESD	HBM	-2000	2000	V	/
ESD	CDM	-500	500	V	/
ESD	Latch up	-200	200	mA	105°C

7.2 Transient Maximum Ratings

Table 7-2 Transient Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Condition
V_CORE	LDO_C input voltage	-0.6	3.0	V	/
V_RF	LDO_RF input voltage	-0.6	3.0	V	/
V_IO	IO, LDO_X and AON PSW input voltage	-0.6	5.0	V	/
V_BACK	AON PSW input voltage	-0.6	5.0	V	/
V_DET_OUT	Antenna detection output voltage	-0.6	5.0	V	/
Vi_{tcxo}	TCXO_IN input voltage	-0.6	LDO_X + 0.6	V	/
Vi_{ana}	RTC_I input voltage	-0.6	V_IO/ V_BACK + 0.6	V	/
Vi_{dig}	PIO 0-9 and RESET_N input voltage	-0.6	V_IO + 0.6	V	/

7.3 Operating Conditions

Table 7-3 Operating Conditions

Symbol	Parameter		Min.	Typical	Max.	Unit
V_CORE	LDO_C input voltage		1.2	1.8	1.98	V
V_RF	LDO_RF input voltage		1.2	1.8	1.98	V
V_IO	IO, LDO_X and AON PSW input voltage		1.7	3.3	3.6	V
V_BACK	AON PSW input voltage		1.7	3.3	3.6	V
V_DET_OUT	Antenna detection output voltage		2.7	3.3	3.6	V
V_DET_IN	Antenna detection input current	Unconnected	/	/	0.5	mA
		Uncertain State	0.5	/	4	

Symbol	Parameter		Min.	Typical	Max.	Unit
		Connected	4	/	60	
		Uncertain State	60	/	80	
		Short circuit	80	/	/	
ILDO_X	LDO_X output current		/	/	5	mA
LDO_X[1]	LDO_X output voltage (using 26 MHz TCXO)		1.78	1.85	1.92	V
LDO_RF[2]	LDO_RF output voltage		0.97	1.0	1.03	V
LDO_C[3]	LDO_C output voltage		0.88	0.92	0.96	V
LDO_RET	LDO_RET output voltage		0.87	0.9	0.93	V
I_{PPS}[4]	PPS output current		/	/	4	mA
T_{amb}	Ambient temperature	UC7510I	-40	+25	+85	°C
		UC7510A	-40	+25	+105	
F_{ref}	Reference clock input at TCXO_IN		/	26	/	MHz

Note: The voltage ranges of V_CORE, V_RF, V_IO, V_BACK and V_DET_OUT have included the voltage ripple.

[1] When V_IO = 1.8 V, it is highly recommended to use an external low-noise LDO to supply power.

[2, 3] If external voltage supply is needed, please contact Unicore Communications, Inc.

[4] Tested without external resistors to prevent reverse current.

7.4 RTC Parameters

Table 7-4 RTC Parameters

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
RTC_F_{xtal}	RTC crystal resonant frequency	/	/	32768	/	Hz
RTC_T_{start}	RTC OSC startup time	/	/	0.2	1	s
RTC_Amp	RTC OSC oscillation amplitude	ESR = 80 kΩ	50	180	350	mVpp
RTC_ESR	RTC crystal equivalent series resistance	/	/	/	90	kΩ
RTC_CL	RTC integrated load capacitance (I/O single-end to the ground)	ESR = 80 kΩ	1	16	31	pF
RTC_V_{pp}	Peak-to-peak voltage of the RTC external digital signal input	/	2	/	Min (V_IO, V_BACK)[1]	V

[1] The voltages of V_IO and V_BACK need to be higher than 2 V.

7.5 RF Parameters

Table 7-5 RF Parameters

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
F_{in}	Receiver input	/	1550	1575.42	1620	MHz

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
	frequency					
LNA_Z_{RFIN}	LNA input impedance	Require matching components and DC blocking capacitors	/	50	/	Ω
LNA_S11	LNA input return loss	50 Ω environment	/	-10	/	dB
NF_{tot}	Receiver chain noise figure	50 Ω environment	/	4	/	dB
Ext_Gain	External gain before matching	50 Ω environment	/	/	55	dB
TCXO_Freq	TCXO frequency	/	/	26	/	MHz
TCXO_V_{pp}	TCXO input peak-to-peak voltage	/	0.5	1.0	1.7	V_{pp}

7.6 PIO Specifications

Table 7-6 PIO Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{leak}	Leakage current input pins	/	/	/	5	uA
V_{il}	Low level input voltage	/	/	/	0.2 × V_IO	V
V_{ih}	High level input voltage	/	0.8 × V_IO	/	/	V
V_{ol}	Low level output voltage	I_{out} = -5 mA	/	/	0.4	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{oh}	High level output voltage	I_{out} = 5 mA	V_IO - 0.55	/	/	V
R_{pu}	Pull-up resistance	/	200	260	320	kΩ
Cap_DIG_IN	Input capacitance of digital IO	/	/	0.7	/	pF

Note: The PIO output type is push-pull.

7.7 Typical Power Consumption

The table below lists examples of the typical current, including RF and baseband section, in GNSS multi-system joint positioning mode. These values are provided for customer reference only. The actual current depends on the firmware version, external circuitry, number of satellites tracked, signal strength, type and time of start, duration, and test conditions.

Table 7-7 Typical Current

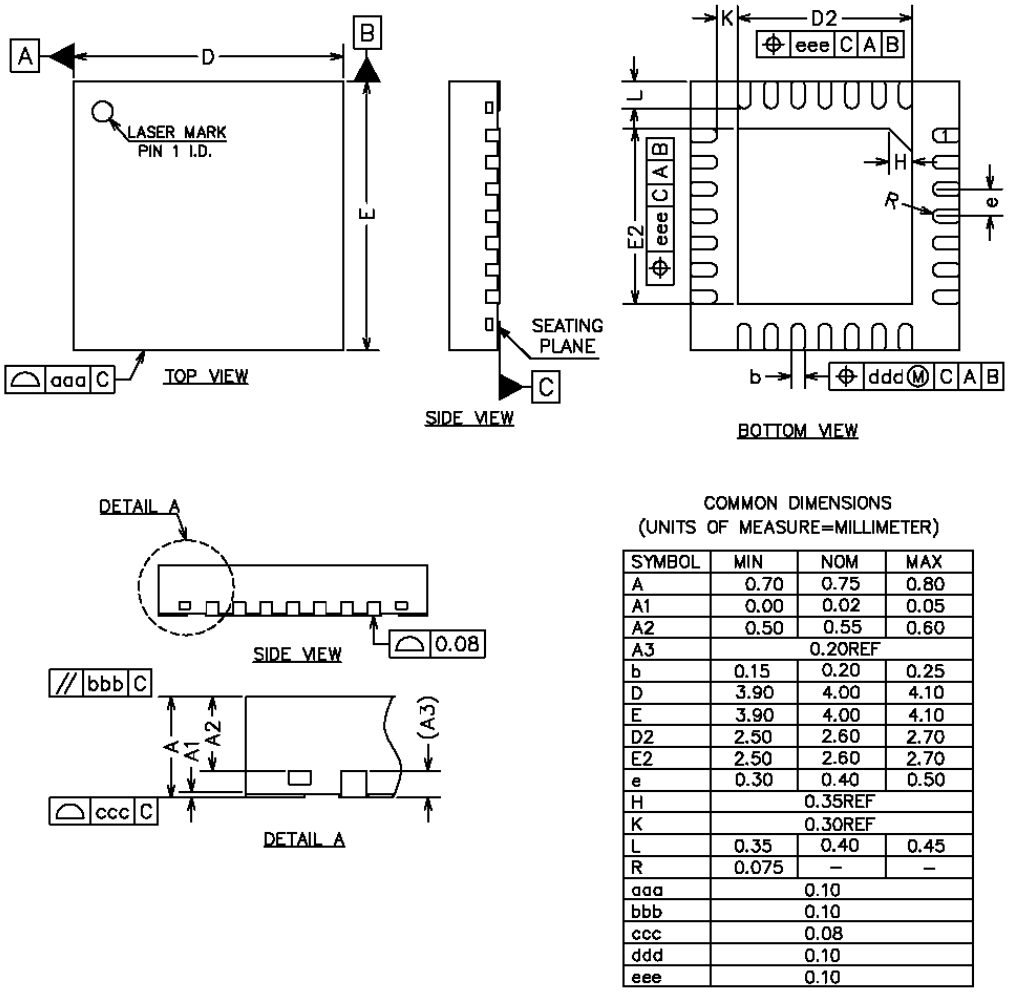
Symbol	Parameter	Condition	Typ.	Unit
I_{V_IO}	Current at V_IO	/	2	mA
I_{V_CORE} & I_{V_RF}	Current at V_CORE and V_RF[1]	Acquisition	48	mA
		Tracking	53	mA
I_{V_BACK}	Current at V_BACK	V_IO power down	7	μA

Note:

- The above currents do not change with the voltages, so the power consumption can be reduced by lowering the voltages.
- The current at V_IO includes currents flowing into the TCXO.
- The test ambient temperature is 25 °C.

[1] The typical acquisition and tracking current of the low-power version is 35 mA and 25 mA respectively.

8 Mechanical Specifications



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.30	0.40	0.50
H		0.35REF	
K		0.30REF	
L	0.35	0.40	0.45
R	0.075	–	–
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

Figure 8-1 QFN28 Mechanical Specifications

9 Reliability Tests and Approvals

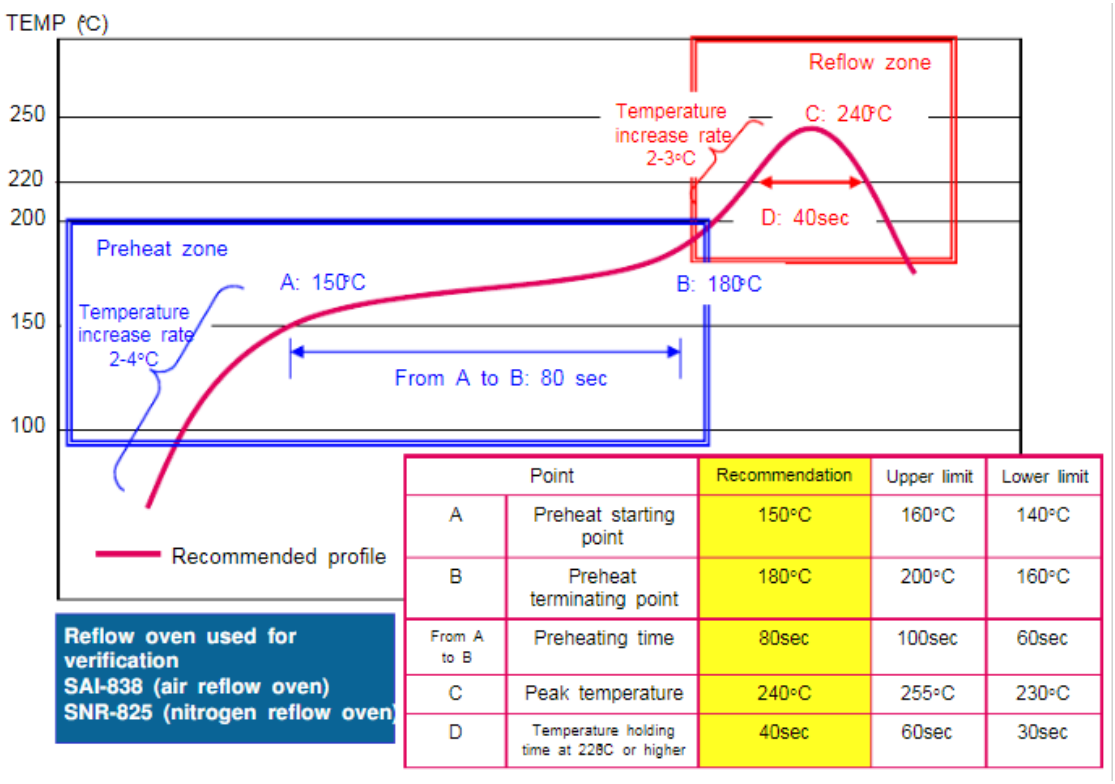
The UC7510 chips meet international standards in terms of reliability testing and environmental protection. For detailed information, please refer to Reliability Tests and Approvals.

Table 9-1 Reliability Tests and Approvals

QualificationTypes		UC7510A	UC7510I
Reliability Tests	JESD47		√
	AEC-Q100 (Grade 2)	√	
Approvals	RoHS	√	√
	REACH	√	√
	CE	√	√
Manufacturing	IATF 16949	√	√
Moisture Sensitivity Level	MSL	MSL 1	MSL 3

10 Reflow Soldering

The reflow soldering temperature curve is recommended as shown in the Reflow Soldering Temperature Curve below (M705-GRN360 is recommended for solder paste).



Point		Recommendation	Upper limit	Lower limit
A	Preheat starting point	150°C	160°C	140°C
B	Preheat terminating point	180°C	200°C	160°C
From A to B	Preheating time	80sec	100sec	60sec
C	Peak temperature	240°C	255°C	230°C
D	Temperature holding time at 228C or higher	40sec	60sec	30sec

Figure 10-1 Reflow Soldering Temperature Curve

11 Product Appearance and Packaging

11.1 Appearance

Figure 11-1 QFN Product Appearance

The appearance of the UC7510 chip is shown in the picture above, and the marking information varies according to the customer's order code. Please follow the actual order.

11.2 Label

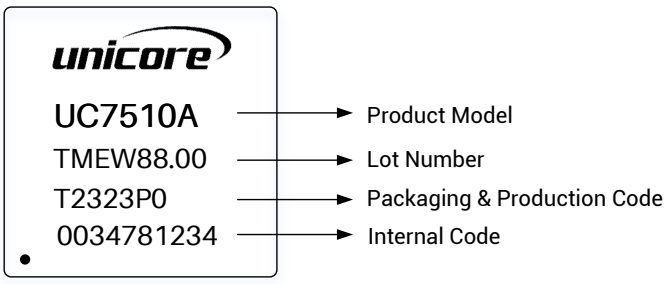


Figure 11-2 UC7510 Product Label

Table 11-1 Label Description

Code	Description
UC7510A	Main model of the product; A = Automotive; I = Industrial
TMEW88.00	Lot number
T2323P0	Packaging and Production Code
0034781234	Internal code

11.3 Packaging

UC7510 chips adopt QFN28 package and are delivered in reeled tapes. Each reel contains 3000 pieces of chips. The package diagram is shown as follows:

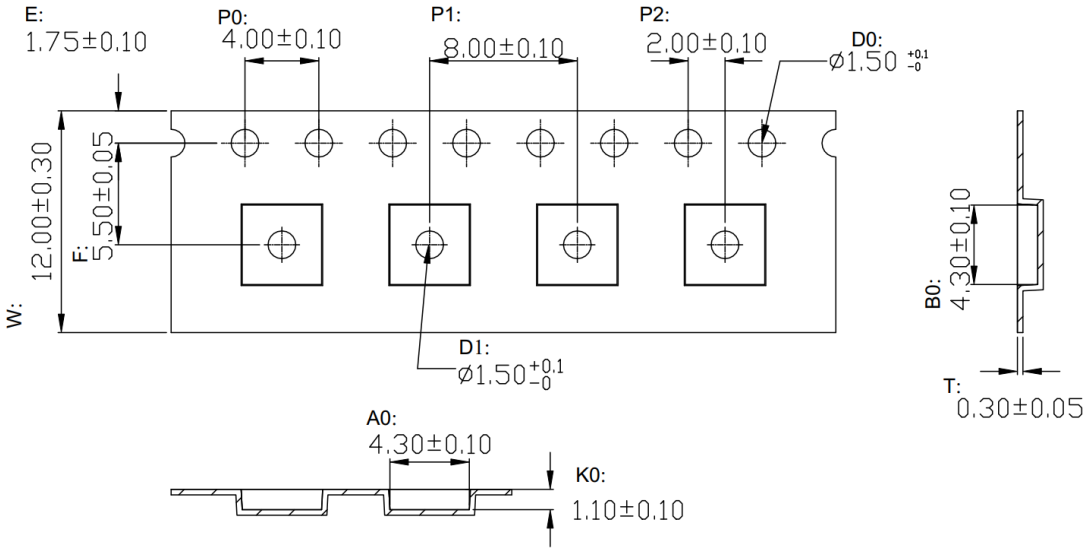


Figure 11-3 UC7510 Tape Dimensions (mm)

The tape dimensions are as follows:

- 10 sprocket hole pitch cumulative tolerance is ± 0.20 mm;
- All dimensions meet EIA-481 requirements;
- Thickness: 0.30 ± 0.05 mm.

12 Ordering Information

Table 12-1 Ordering Information

Product	Description
UC7510I	QFN28 package, industrial grade, built-in Flash, supports firmware upgrade.
UC7510A	QFN28 package, automotive grade, compliant with AEC-Q100 (Grade 2), built-in Flash, supports firmware upgrade.

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